A-SSCC 2016 Reports Program (2016/11/11)

Session Chair	Time		Title	Speaker(Affiliation)
Professor Ikeda (University of Tokyo)	13:00 13:15	S21-1	A 2nd Order Fully-Passive Noise-Shaping SAR ADC with Embedded Passive Gain	Masaya Miyahara (Tokyo Institute of Technology)
	13:15 13:30	S3-1	A 3.2 mA-RX 3.5 mA-TX Fully Integrated SoC for Bluetooth Low Energy	Masayoshi Oshiro (Toshiba)
	13:30 13:45	S3-2	A 2GS/S 8b Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC	Takuji Miki (Panasonic)
	13:45 14:00	S3-3	20mV Input, 4.2 V Output SIDO Boost Converter with Low-Power Controller and Adaptive Switch Size Selector for Thermoelectric Energy Harvesting	Yosuke Toyama (Toshiba)
	14:00 14:15	S3-5	A 5.92-Mb/mm2 28-nm Pseudo 2-Read/Write Dual-Port SARM Using Double Pumping Circuitry	Yuichiro Ishii (Renesas Electronics)
	14:15 14:30	S4-2	Time-Domain Neural Network: a 48.5 TSOp/s/W Neuromorphic Chip Optimized for Deep Learning and CMOS Technology	Daisuke Miyashita (Toshiba)
	14:30 15:00		Break	
Professor Ito (Tokyo Institute of Technology)	15:00 15:15	S4-6	An Inductive-Coupling Bus with Collision Detection Scheme Using Magnetic Field Variation for 3-D Network-on-Chips	Junichiro Kadomoto (Keio University)
	15:15 15:30	S5-2	56-Level Programmable Voltage Detector in Steps of 50mV for Battery Management	Teruki Someya (University of Tokyo)
	15:30 15:45	S6-1	A 9-Bit 500-MS/s 6.0-mW Dynamic Pipelined ADC Using Time-Domain Linearized Dynamic Amplifiers	Yu Lian (Tokyo Institute of Technology)
	15:45 16:00	S8-2	An Lo-Buffer-Less 60-GHz CMOS Transmitter with Oscillator Pulling Mitigation	Wu Rui (Tokyo Institute of Technology)
	16:00 16:15	S16-1	All-Digital Single-Inductor Multiple-Output DC-DC Converter with Over 65.3% Efficiency in 1 uW to 50 mW Load Range and 86.3% Peak Efficiency	Manabu Yamada (Toshiba)
	16:15 16:30	S16-4	A 0.38-uW Stand-by Power, 50-nA-to-1-mA Load Current Range DC-DC Converter with Self-Biased Linear Regulator for Ultra-Low Power Battery Management	Toshiro Ozaki (Kobe University)
	16:30 17:00		Break	
Takeshi Yamamura (Fujitsu Laboratories)	17:00 18:00		Design of PLLs with Binary Phase Detectors for Frequency Synthesis & CDR	Asad Abidi (UCLA)

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